ABSTRACT OF THE DISCLOSURE

This data processor can satisfy both requests of a fast transition from a low power consumption state to an operating state and low power consumption, and a data processor has a program running state, a standby mode, a light standby mode, and a sleep mode. In the sleep mode, the supply of a synchronizing clock signal to a central processing unit (CPU) is stopped and the synchronizing clock signal is supplied to other circuit modules. In the standby mode, the frequency multiplication and frequency operation of a clock pulse generator are suspended and the supply of the synchronizing clock signal to the CPU and other circuit modules is stopped. In the light standby mode, the frequency multiplication and frequency division operation of the clock pulse generator are enabled and the supply of the synchronizing clock signal to the CPU and other circuit modules is stopped. In the light standby mode, the transition of the CPU to an instruction executable state is faster than in the standby mode and the lower power consumption than in the sleep mode is obtained.